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BUFDNI103 Datasheet

Overview

The BUFDNI103 provides three buffer channels having both non-inverting and inverting logic-level outputs. Input logic signals as high as 15.25V may be applied directly, and the design includes provisions for the user to easily add their own divider resistors which allow higher input voltages to be applied if needed. The output-side power supply (VCC), which sets the logic level of the outputs, may be set to a voltage anywhere from 2V to 6V. In addition to the capability to simply act as a buffer (inverting and non-inverting), this configuration makes the BUFDNI103 perfect for down-conversion logic-level translation (higher logic-level voltage down to a lower logic-level voltage). Fast rise and fall times on the outputs are accomplished with a buffer IC that has push-pull outputs. Terminal blocks provide easy access to the signals while maintaining a compact form factor.

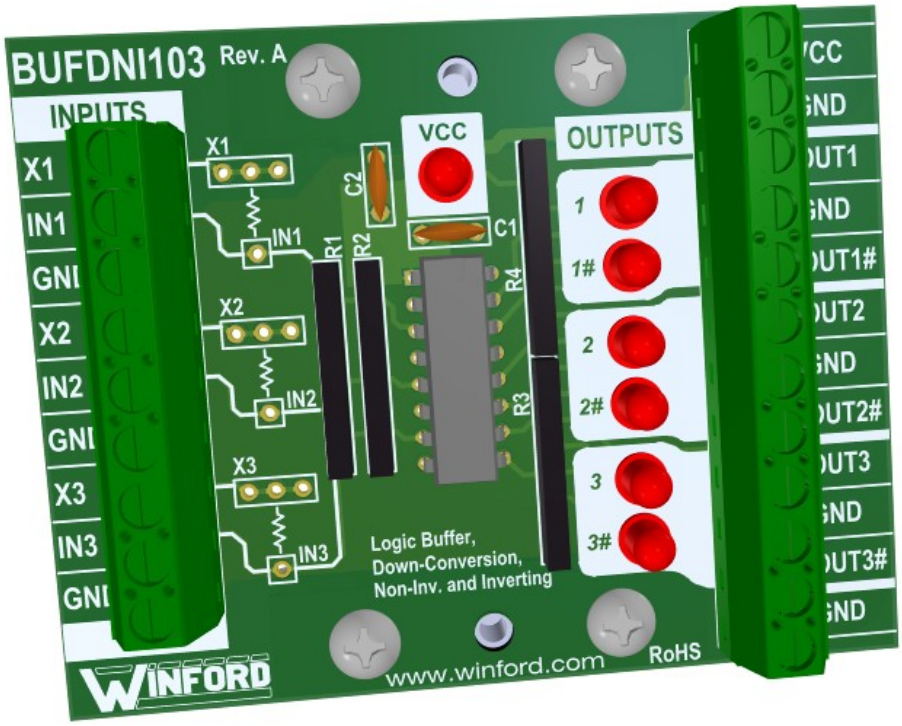


Figure 1

Dimensions (typical shown)

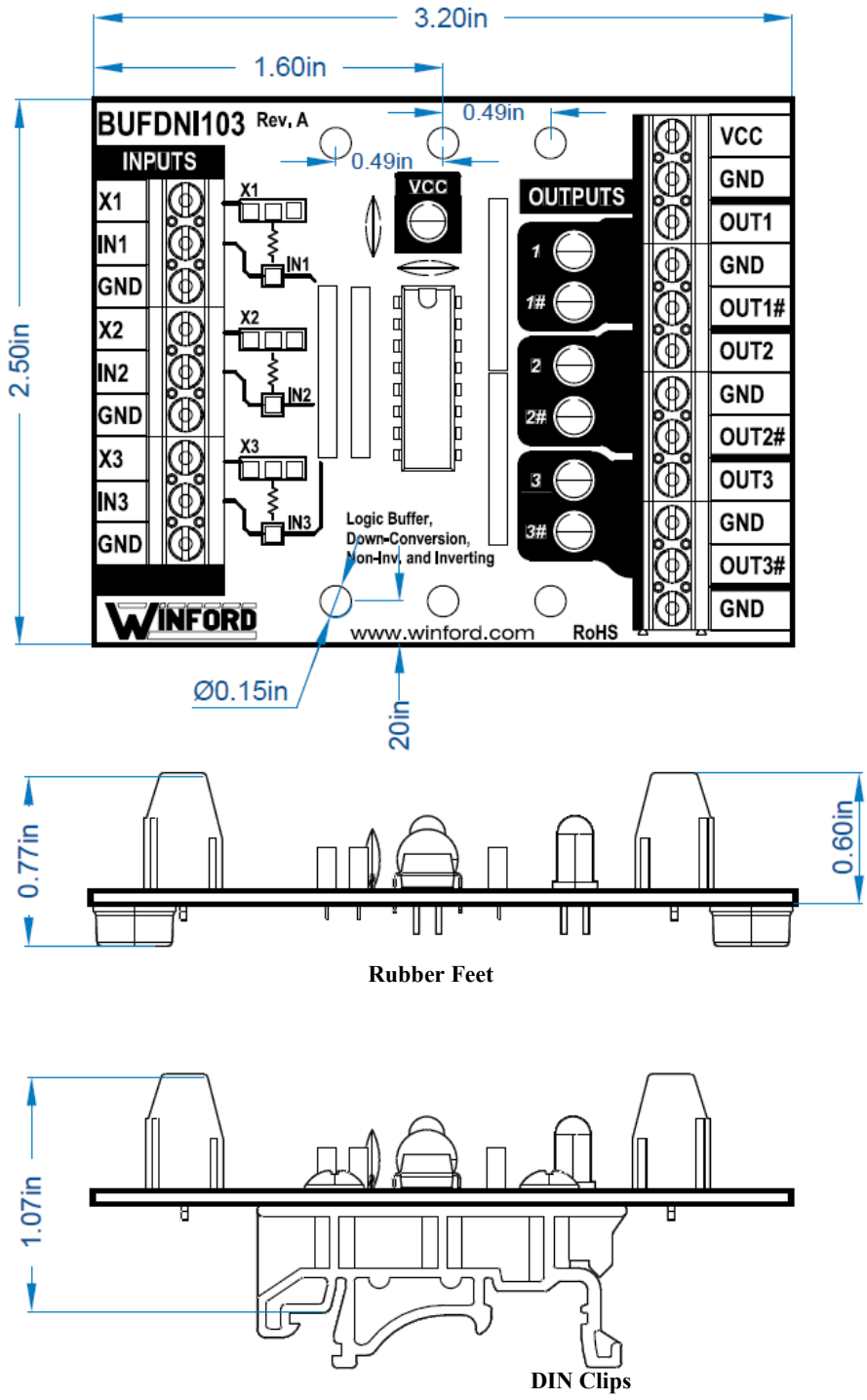


Figure 2

Part Number Ordering Information

BUFDNI103	-	
		1

1. Mounting Option

- **FT** Rubber Feet on bottom side of PCB
- **DIN** DIN Rail Mounting Clips

Simplified Schematic Drawing (one channel)

Implementation is the same for all channels.

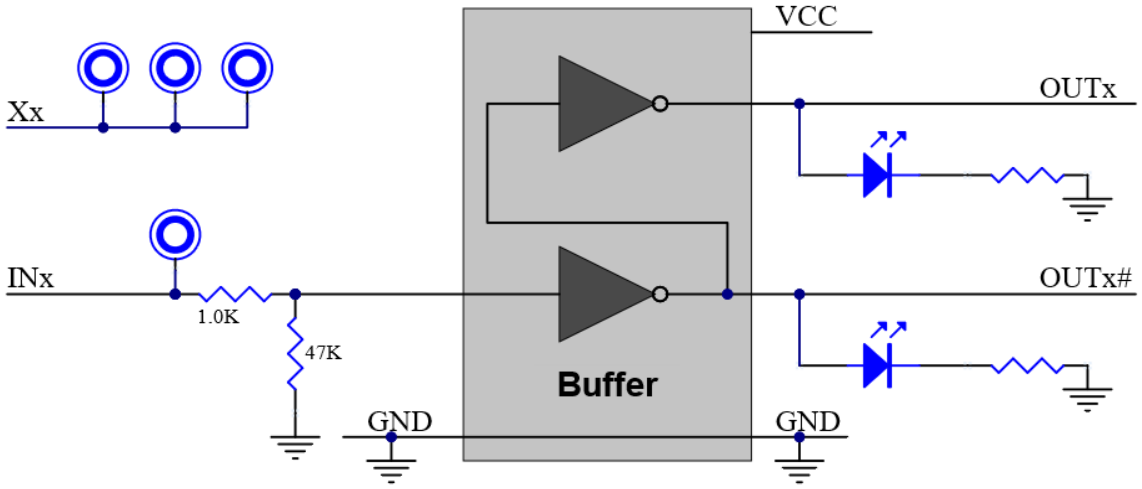


Figure 3

Although both non-inverting and inverting outputs are provided for each signal, these outputs are not exactly differential signals, strictly speaking. The non-inverting output is slightly delayed relative to the inverting output. See the timing section in this document for more information.

As shown in the simplified schematic, both the input and output circuitry share a common ground.

Detailed Description

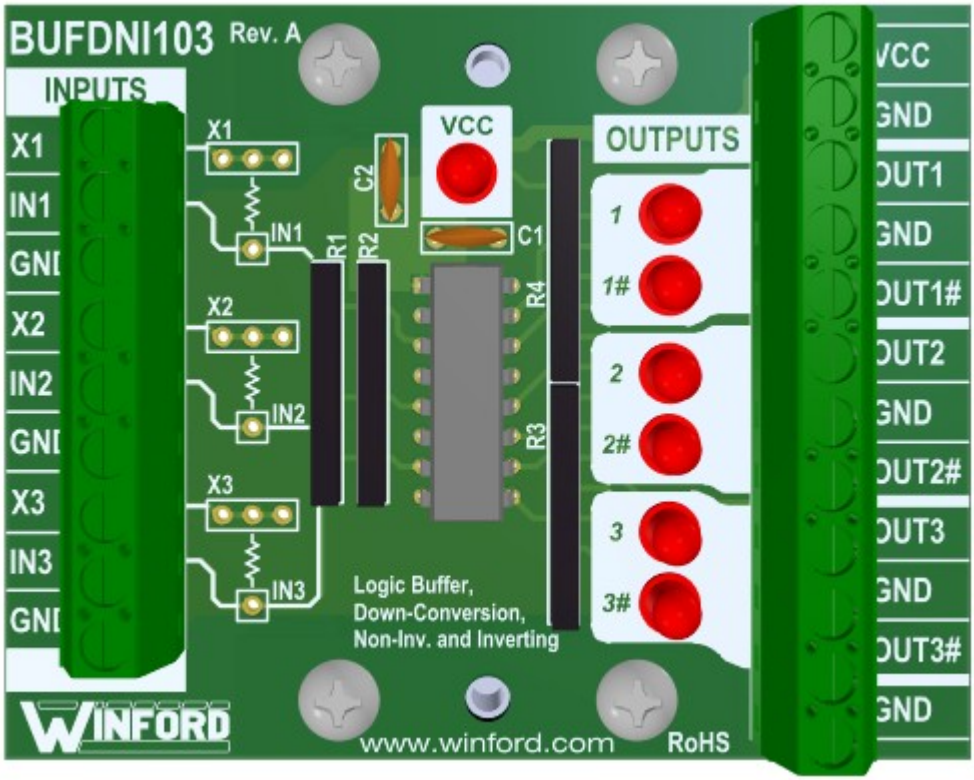


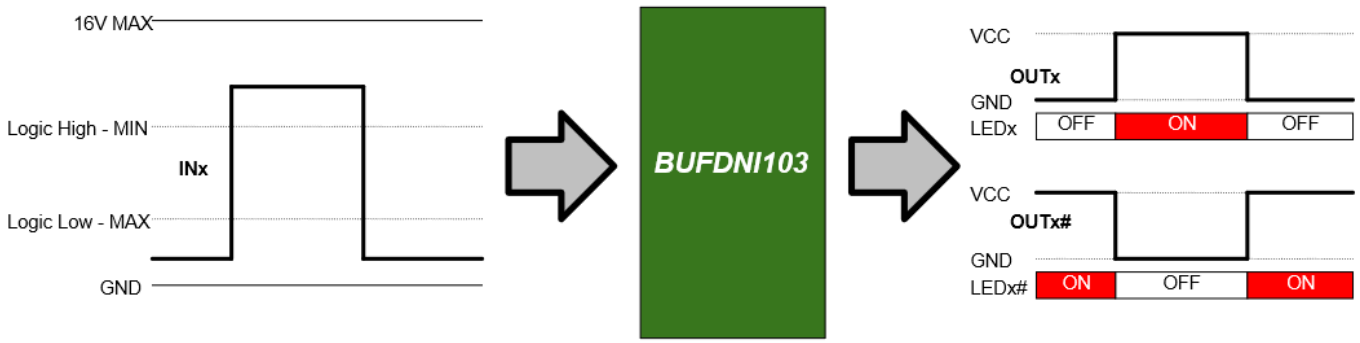
Figure 4

SIGNAL	DESCRIPTION
Xx	Extra uncommitted inputs tied to thru-hole pads on the PCB. See applications section.
INx	Input signal for Channel x
GND	Ground reference

SIGNAL	DESCRIPTION
VCC	Output-side Supply Voltage
OUTx	Non-inverting output for Channel x
OUTx#	Inverting output for Channel x
GND	Ground reference

Note that all GND positions (both input side and output side) are connected together on the PCB. Thus, the signals connected to the input side and the output side must all share a common ground reference.

The following figure illustrates the functional behavior of this device. On each channel, two LEDs provide a visual indication of the non-inverting and inverting output states. An LED that is lit indicates that the given output is high.



Output Signal and LED Indicators vs Input Signals

Figure 5

As indicated in the figure, the logic-high voltage level of the output signals depends on the output-side supply voltage, VCC. It is also important to note that the logic-high/low threshold voltages on the input side also depend on the value of VCC. The table below provides the input-side logic thresholds that must be observed as a function of the VCC supply voltage.

Output-Side VCC Supply Voltage	Min Input Signal Required for Logic High	Max Input Signal Allowed for Logic Low
6.0V	4.3V	1.8V
5.0V	3.6V	1.5V
4.5V	3.3V	1.3V
3.3V	2.6V	0.8V
3.0V	2.3V	0.7V
2.5V	2.0V	0.6V
2.0V	1.6V	0.5V

Table 1

Example 1: If you want the output signals to be 5V logic, then set VCC to 5V. For this value of VCC, any input above 3.6V will be interpreted as a logic high, and any value below 1.5V will be interpreted as a logic low.

Example 2: If you want the output signals to be 3.3V logic, then set VCC to 3.3V. For this value of VCC, any input above 2.6V will be interpreted as a logic high, and any value below 0.8V will be interpreted as a logic low.

(Note: The guaranteed min/max thresholds are shown in Table 1. The typical switch-point thresholds will be somewhere between the guaranteed min and max thresholds.)

Operating Conditions

Ambient Temperature Range	–30°C to 85°C
Relative Humidity Range - not icing or condensing	5% to 85% RH

Absolute Maximum Ratings (25 degC, all voltages relative to GND)

Specification	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Supply Voltage	VCC	-0.5		7.0	V
Input Signal Voltages	V_INx	-15		16	V
Output Signal Voltages	V_OUTx	-0.5		VCC+0.5	V
Output Signal DC Source or Sink Current	I_OUTx	-20		20	mA

Exceeding the absolute maximum ratings may result in damage to the product.

Electrical Performance and Recommended Operating Conditions (at 25 degC, all voltages relative to GND)

Specification	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Supply Voltage	VCC	2.0		6.0	V
Supply Current, no external loading on output signals VCC=3.3V VCC=5.0V VCC=6.0V	ICC		 4 9 11		mA
Input Signal Voltage Range	V_INx	0		15.25	V
Input Logic Threshold Voltages	V_IH, V_IL	See Table 1 on page 5			V
Input Signal Transition Time req't (rising or falling)* VCC = 2.0V VCC = 4.5V VCC = 6.0V *See appendix for more information on this parameter	t_r, t_f			 1000 500 400	ns
Input Signal Current V_INx = 3.3V V_INx = 5.0V V_INx = 12V V_INx = 15V	I_INx		 0.07 0.10 0.25 0.31		mA
Output Signal Voltages, Logic High VCC = 3.3V, Load = 10k to ground VCC = 5.0V, Load = 10k to ground VCC = 6.0V, Load = 10k to ground	V_OUTHx		 3.2 4.9 5.9		V

Specification	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Output Signal Voltages, Logic Low VCC = 3.3V, Load = 10k to VCC VCC = 5.0V, Load = 10k to VCC VCC = 6.0V, Load = 10k to VCC	V_OUTLx		 0.02 0.02 0.02		V

Screw Terminal Wire Sizes

- All Signals and Power: 12-30 AWG

Output Stage Component Details

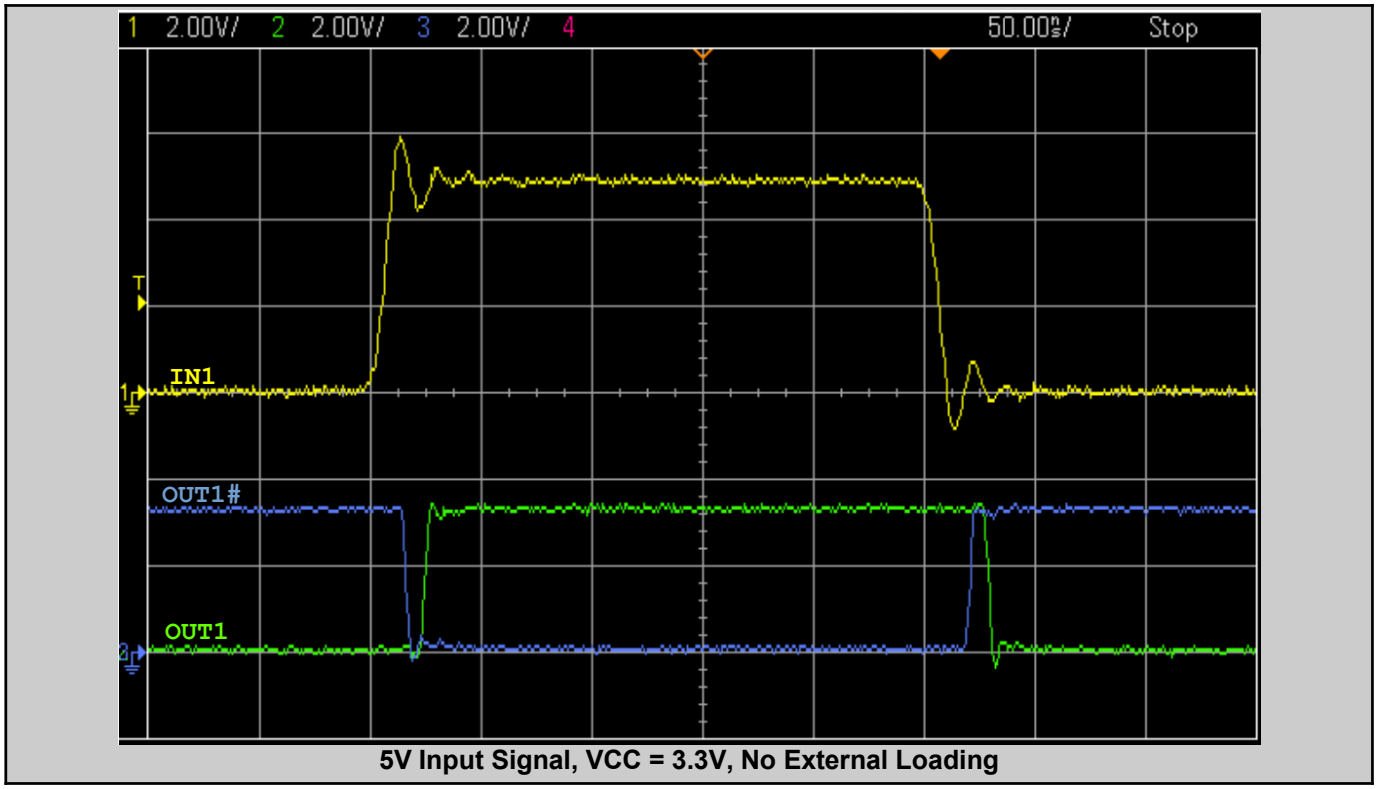
The signal path is provided in the simplified schematic drawing shown previously in this document. Additional information is provided below.

Component	*Manufacturer*	*Manuf. Part Number*
Buffer IC	Texas Instruments	CD74HC4049

Typical Timing Performance

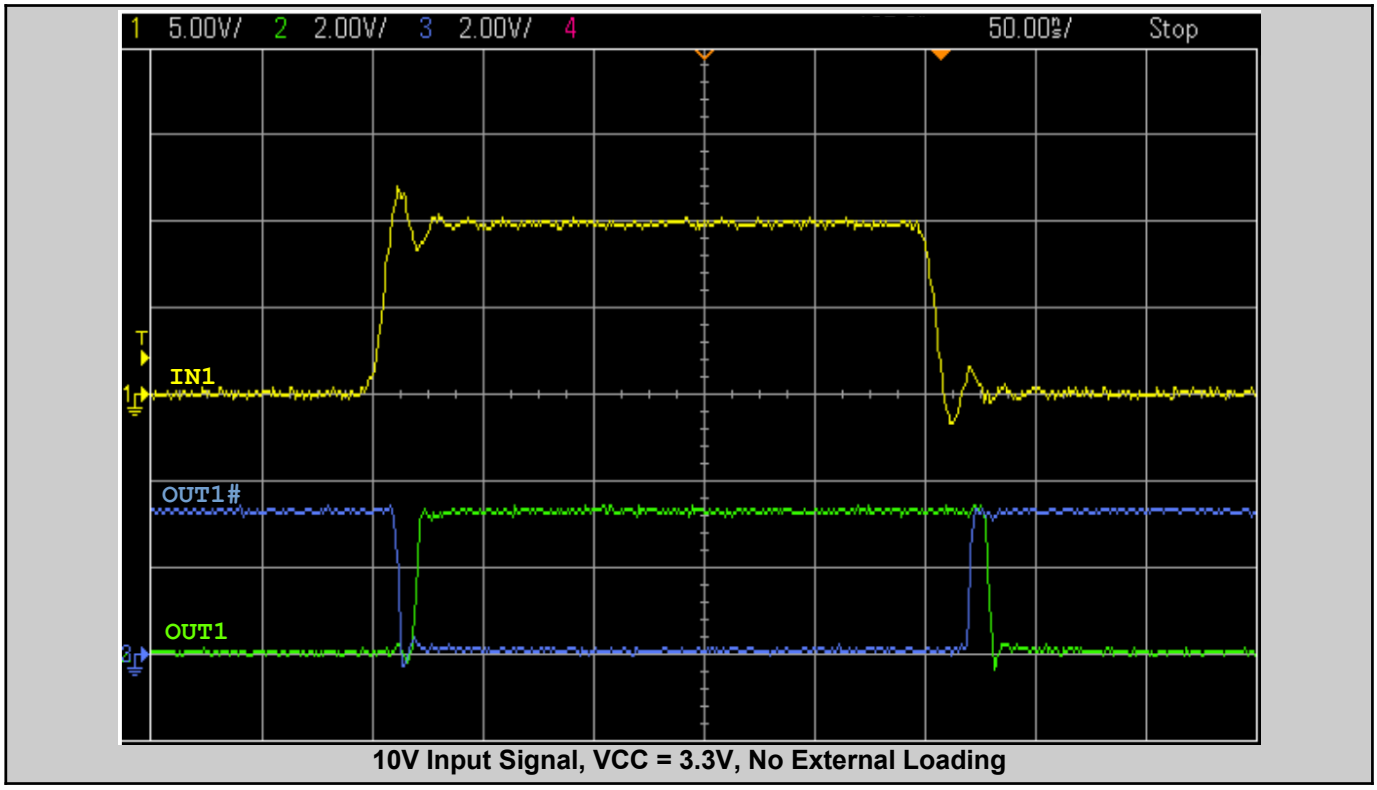
For reference, some typical output transition timing plots are provided on the following pages (for a single channel). In all plots, the horizontal time scale is 50 ns/division.

Case 1: Converting from 5V logic to 3.3V logic



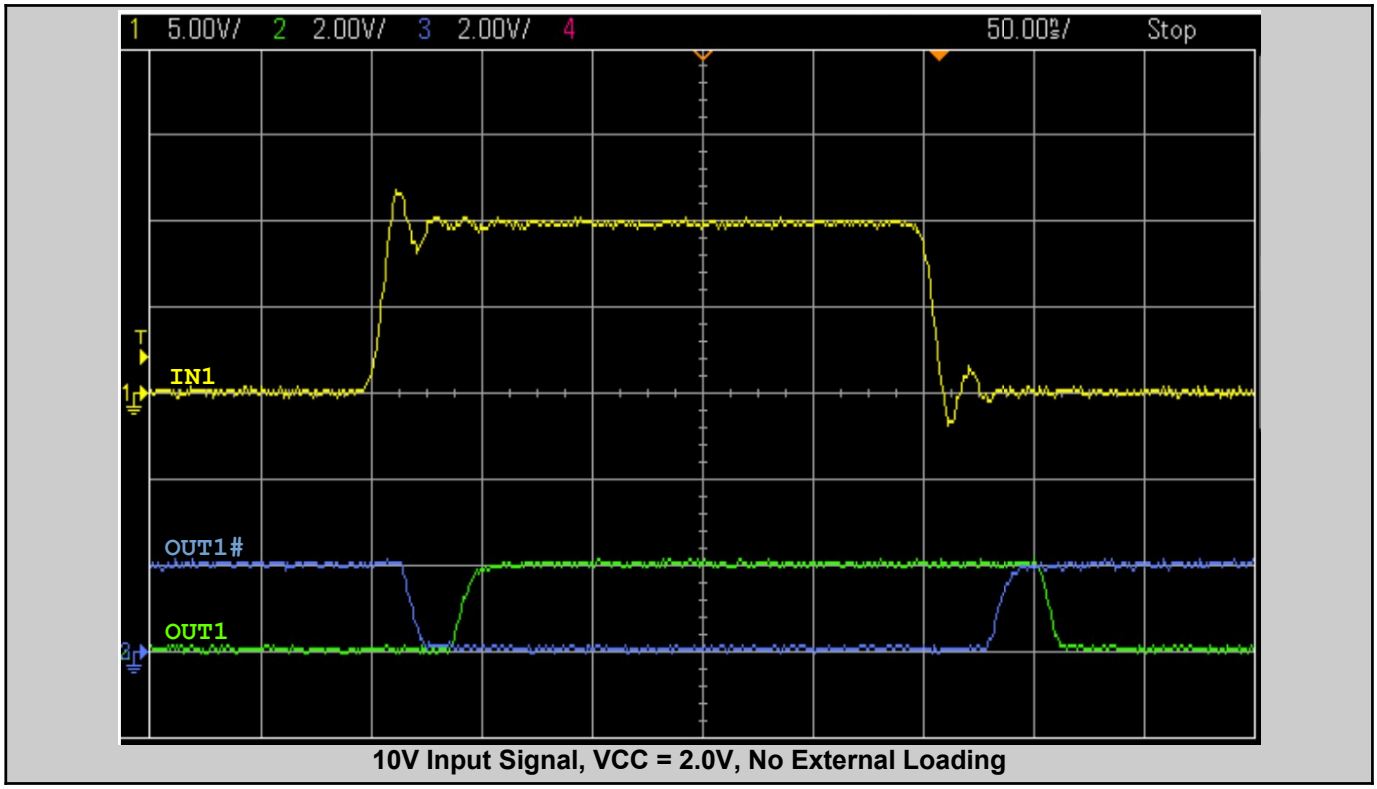
5V Input Signal, VCC = 3.3V, No External Loading

Case 2: Converting from 10V logic to 3.3V logic



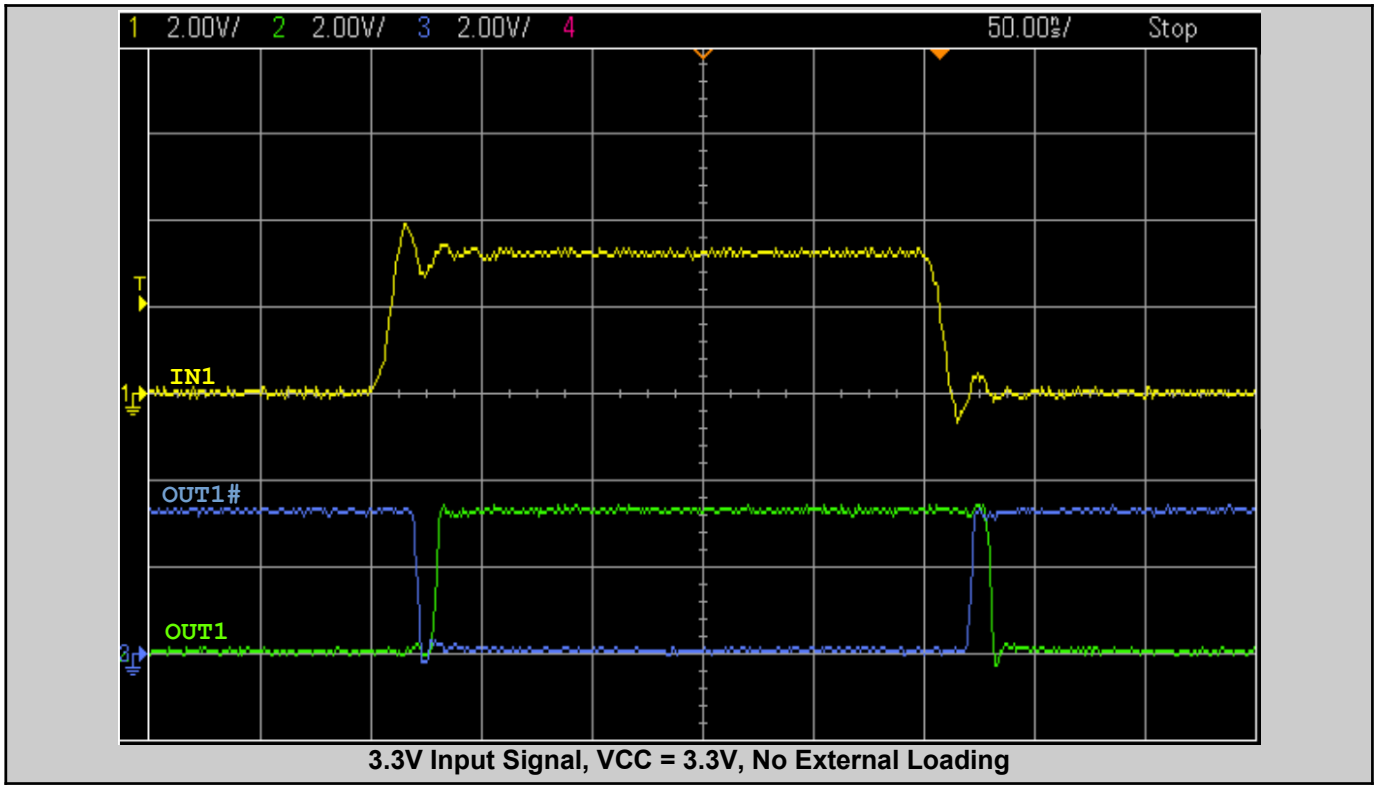
10V Input Signal, VCC = 3.3V, No External Loading

Case 3: Converting from 10V logic to 2.0V logic



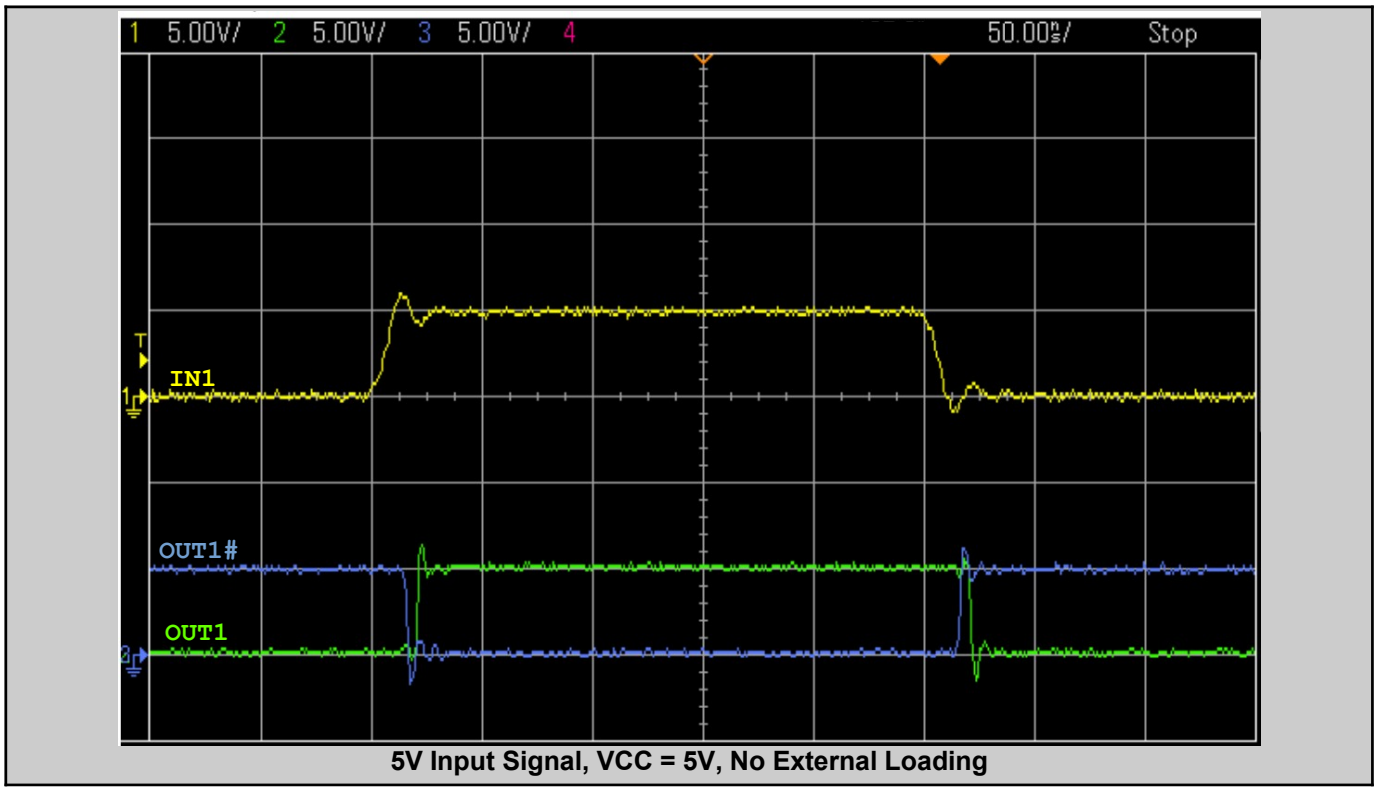
10V Input Signal, VCC = 2.0V, No External Loading

Case 4: Buffering / Inverting: 3.3V logic in, 3.3V logic out



3.3V Input Signal, VCC = 3.3V, No External Loading

Case 5: Buffering / Inverting: 5V logic in, 5V logic out

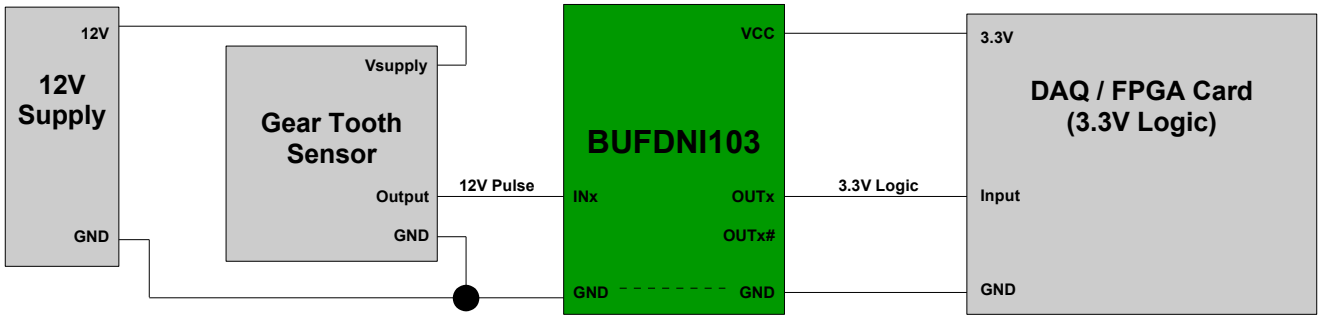


5V Input Signal, VCC = 5V, No External Loading

Applications

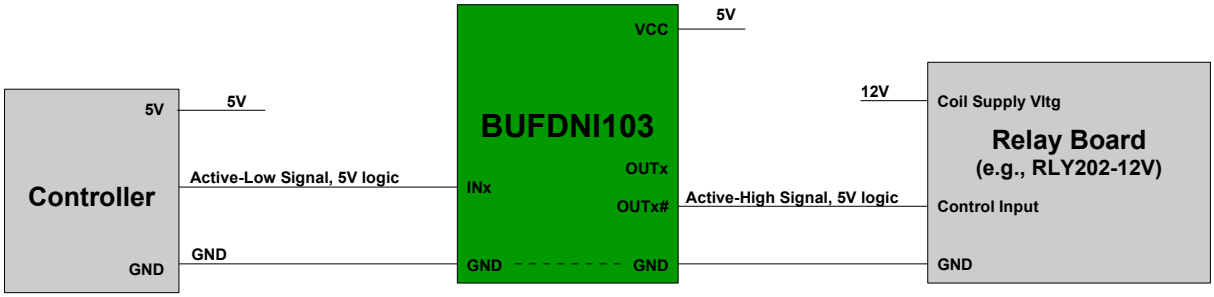
Logic Level Translation for Inputs up to 15.25V

The figure below shows this device being used to convert a 12V gear tooth sensor pulse down to a 3.3V pulse so that the pulse can be measured by a DAQ / FPGA card. In this case, the 3.3V needed for VCC is supplied by the DAQ / FPGA card, but it could just as well come from a separate 3.3V power supply.



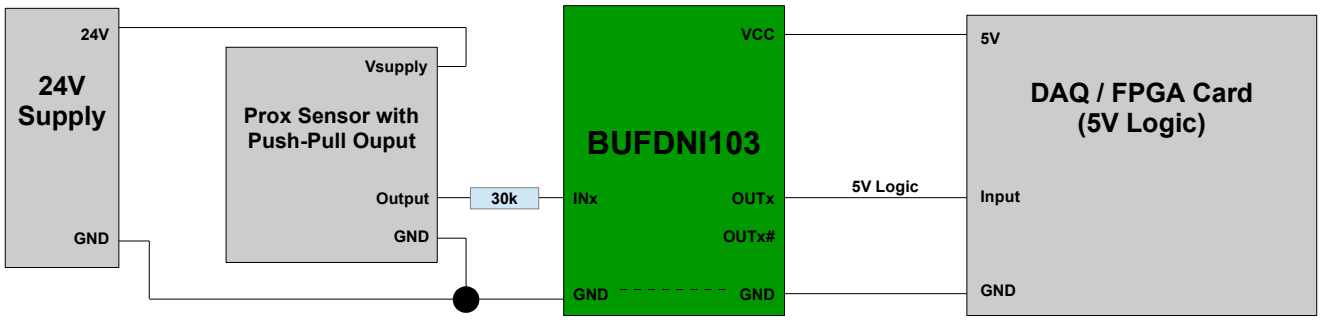
Logic Inversion

The figure below shows this device being used to simply invert a 5V logic control signal, without level-shifting. In this case, an active-low signal is being used to control a relay board that requires an active-high signal to activate the relay.

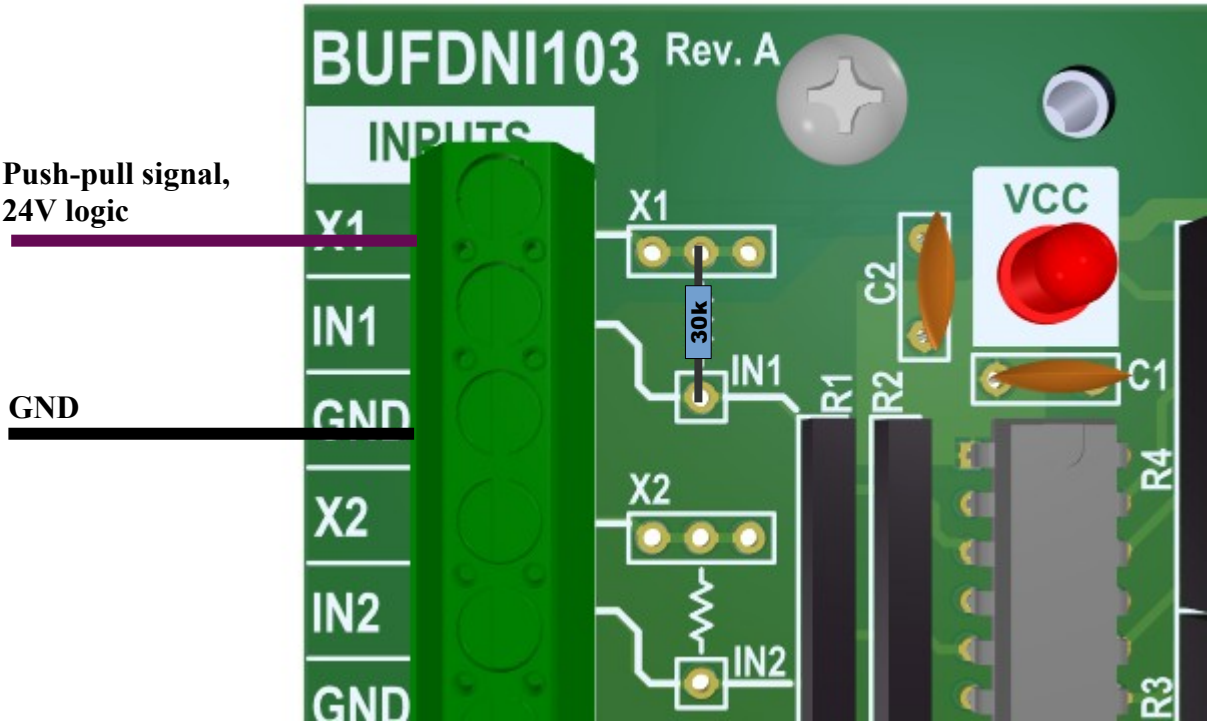


Logic Level Translation for Inputs Greater than 15.25V, Coming from a Sensor Push-Pull Output

There may be situations in which this device needs to interface to a sensor signal that is greater than 15.25V. In this case, a series resistor can be added in order to form a divider (along with the pulldown resistor that is already present on each input – See Figure 3). The figure below shows this device along with an external series resistor being used to convert a 24V signal down to a 14.V signal (approximately) which feeds the input. The BUFDNI103 then converts that signal to a 5V signal. In this case, the sensor has a push-pull output.

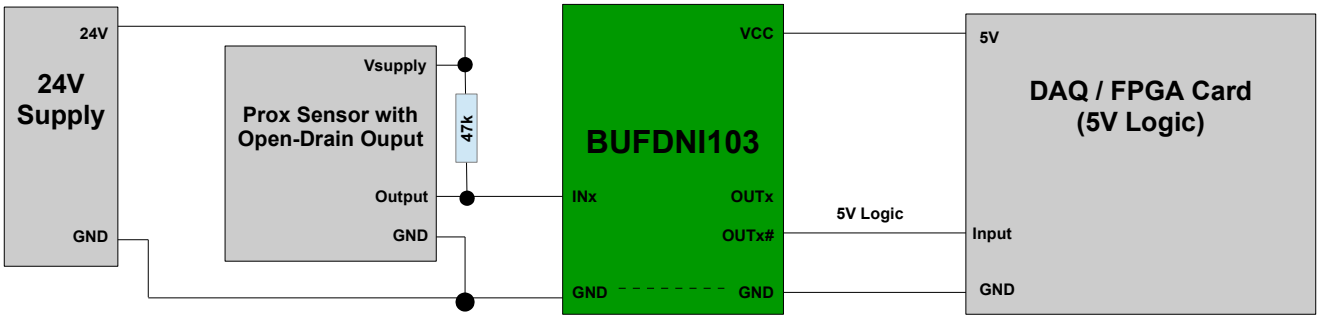


In order to simplify the implementation of this configuration, the BUFDNI103 includes extra input positions (Xx) that are simply connected to thru-hole pads, and also includes a thru-hole pad on each input (INx). For channel 1, for example, the sensor output can be connected to extra input position X1 (instead of IN1), and the 30k resistor can be placed between X1 and IN1 on the BUFDNI103 PCB.

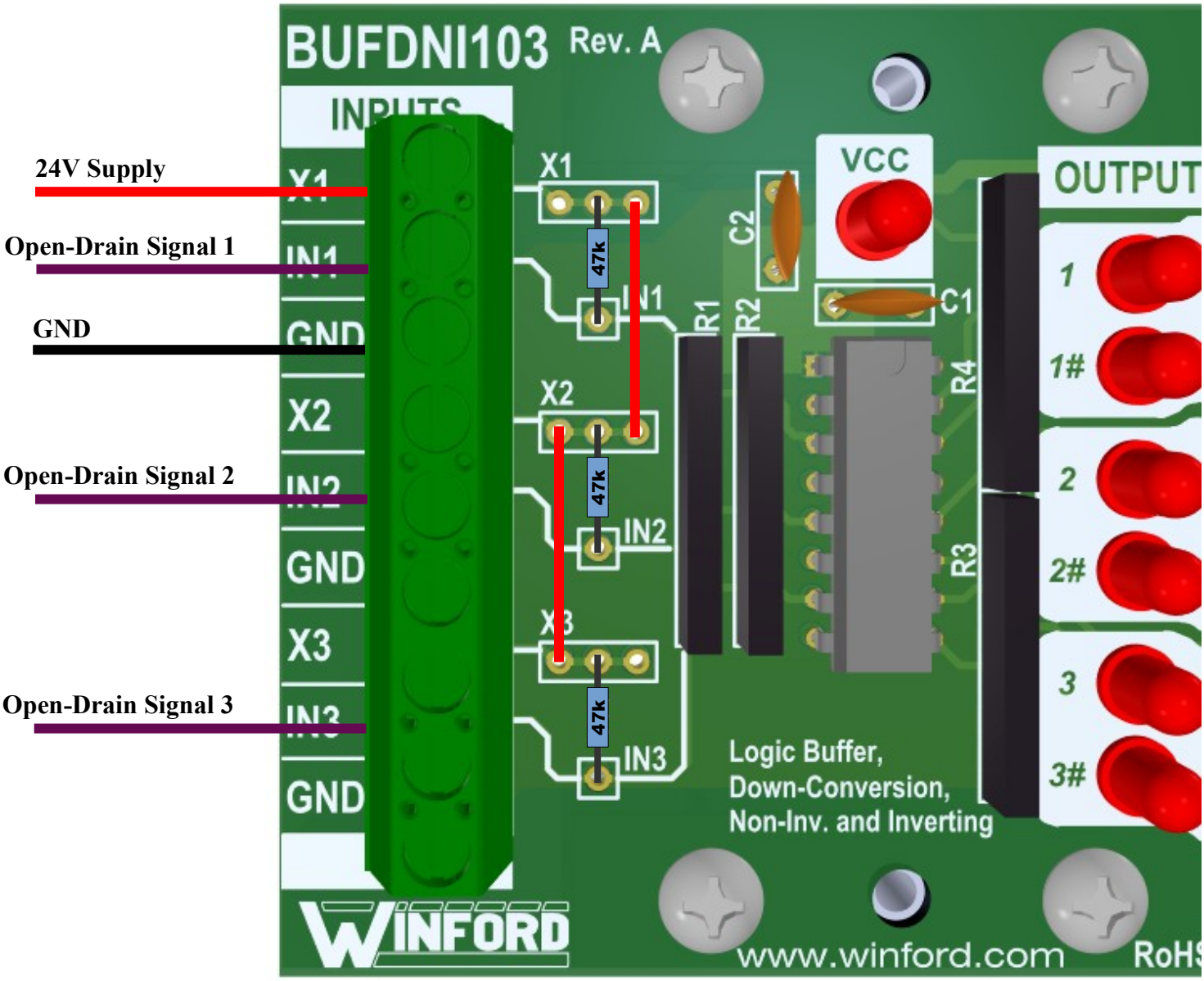


Logic Level Translation for Inputs Greater than 15.25V, Coming from a Sensor Open-Drain Output

In other cases, it may be that the sensor has an open-drain (or open-collector) output. This is very common in sensors. In the case of an open-drain / open-collector output, the sensor can only sink current. That is, the sensor can only pull the output down to ground. In order to get the output to go high, a pullup resistor is needed. Just be aware that the pullup resistor along with the pulldown resistance on this device will form a resistor divider. This is useful when interfacing to a signal that is being pulled up to 24V since the divider can be used to meet the max input voltage limitation of 15.25V. This is illustrated in the figure below, in which a signal from a 24V open-drain sensor is converted to 12V logic (approximately) which feeds the input. That signal is then converted to 5V inverted logic by the BUFDNI103.



Like the previous example, the extra input positions and thru-hole pads can be used to simplify the implementation of this configuration. Consider the case in which all 3 inputs are connected to open-drain signals, and the pull-up supply rail is 24V. The 24V rail can be connected to one of the extra inputs, and wire jumpers can be added by the user (on the PCB) to connect the 24V rail to the other extra inputs (using the thru-hole pads). Then, the 47k pullup resistors can be added to the PCB, connected between each input and 24V.



System Analysis: Failure Modes & Effects

When designing any system, it is advisable to ensure that there is a thorough understanding of what will happen when each piece of the system fails. It is the responsibility of the system designer to ensure that the failure effects are understood, and that appropriate countermeasures or redundancies are implemented if warranted.

If there are additional questions about using this product in a particular application, please contact Winford Engineering for more information.

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Appendix

Max allowed input signal transition time is a parameter that is often overlooked, but it is a common limitation on logic gate ICs (unless they include Schmitt trigger inputs). As the input signal is transitioning from high to low or from low to high (in the indeterminate region), there is a point at which the high-side FET and the low-side FET in the push-pull output may both be partially on at the same time, resulting in shoot-thru current, and possibly output oscillation. The spec on max allowed transition time ensures that the device passes thru this specific operating point very quickly, guaranteeing no degradation to the output stage of the device.

For a more thorough understanding, refer to Texas Instruments application report SCBA004, "Implications of Slow or Floating CMOS Inputs."

Some typical transition times for digital outputs on a few popular products are shown below for reference.

Arduino MEGA2560 (5V logic):	about 4 ns
Arduino UNO (5V logic):	about 4 ns
Arduino DUE (3.3V logic):	about 3 ns
Arduino MKRZERO (3.3V logic):	about 10 ns
Arduino NANO (5V logic):	about 4 ns

As can be seen, these transition times are very small compared to the max allowed input signal transition time on the BUFDNI103, which allows them to be readily used together.